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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,336	11/13/2001	Chaitanya S. Rajguru	10559-519001 / P12423	5776

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EXAMINER
DESTA, ELIAS

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 06/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N . 09/993,336	Applicant(s) RAJGURU, CHAITANYA S.	
	Examiner Elias Desta	Art Unit 2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

Drawing

1. The drawing is objected to because of the following minor informalities:

- Fig. 2: line 23 should be labeled as to its function.
- Fig. 3B: delete "40"
- Fig. 4: elements 47 and 46 should be labeled as to their function.
- Fig. 5: box 46 should be labeled as to its function.

Claim rejection – 35 U.S.C. 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. *Claims 1-25* are rejected under 35 U.S.C. 102(b) as anticipated by *Kawahara et al.* (IEEE Journal).

In reference to claims 1, 7, 13, 19 and 20: *Kawahara et al.* teaches an apparatus for generating an internal voltage for a low voltage flash memories (see *Kawahara et al.*, Abstract). The apparatus includes:

- A charge pump having a capacity that is preset to a particular value (see *Kawahara et al.*, page 126, 1st column, paragraph 3 to 2nd column, paragraph 1, and Fig. 1).

- A measuring circuit to measure the actual capacity of the charge pumps and to reset the capacity of the charge pumps to a value based on the measured capacity (see *Kawahara et al.*, page 129, 1st column, 1st paragraph and Fig. 1, sense and latch circuit).
- An array of memory cell because memory cells in Flash technology is set in an array arrangement (see *Kawahara et al.*, Fig. 1, memory cell).
- It is inherent that the measurement and the analysis in *Kawahara et al.* is done using a computer because in Fig. 1, the decoder is interfaced to an output port which serves for carrying out further analysis as shown in Figs. 9-11.

With regard to claims 2, 8, 14 and 21: as noted above in claims 1, 7, 13 and 20, *Kawahara et al.* further teaches that an output of the charge pump is preset to operate at a particular voltage and current (see *Kawahara et al.*, page 129, Fig. 11 and 1st column, 1st paragraph).

With regard to claims 3, 9, 15 and 22: as noted above in claims 1, 7, 13 and 19, *Kawahara et al.* further teaches that the measuring circuit includes a temperature sensor because the reference voltages are expressed in terms of temperature dependence (see *Kawahara et al.*, page 129, Fig. 9).

With regard to claims 4, 5, 10, 11, 16, 17, 23 and 24: as noted above in claims 1, 7, 13 and 19, *Kawahara et al.* further teaches that the measuring circuit includes voltage sensor to sense a voltage at an input and output of the charge pump (see *Kawahara et al.*, Fig. 1, sense and latch circuit and reference voltage).

With regard to claims 6, 12, 18 and 25: as noted above in claims 1, 7, 13 and 19, *Kawahara et al*. further teaches that the measuring circuit includes a current sensor to sense a current at an output of the charge pump (see *Kawahara et al*., page 129, paragraph 1 and page 130, Fig. 12).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant disclosure.

- *Lee et al*. (U.S. 6,381,670) teaches flash memory array having maximum and minimum threshold voltage detection for eliminating over-erasure problem and enhancing write operation.
- *Lin et al*. (IEEE Journal) teaches a 4-phase charge pumping circuit for low supply voltages using 0.6 μm triple-well CMOS technology to generate high negative boosted voltage.
- *Tanzawa et al.* (IEEE Journal) teaches a stable programming pulse generator for single power supply, high-speed programming and low power Flash memories.
- *Song et al.* (U.S. Patent 5,978,275) teaches the process of erase and program control state-machines for flash memories.
- *Akaogi et al.* (U.S. Patent 6,111,787) teaches a system for generating an address transition signal for a dual bank flash memory device.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Desta whose telephone number is (703)-305-3840. The examiner can normally be reached on M-Thu (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)-308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-308-5841 for regular communications and (703)-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-1782.

Elias Desta
Examiner
Art Unit 2857

-ed

May 22, 2003

HAL WACHSMAN
PRIMARY EXAMINER